COURSE SYLLABUS

Digital Systems Test ECE 6140

Fall 2026

Course description

Study of fault models, test generation, simulation, and design-for-testability (DFT) techniques for digital, memory, and mixed-signal systems. Emphasis on algorithmic foundations (ATPG, simulation) and practical test architectures (scan, BIST, compression), with a semester-long project implementing a fault simulator and test generator.

Learning outcomes

By the end of the course, students will be able to:

1. Model faults and analyze their impact on circuit behavior
2. Develop and evaluate ATPG algorithms
3. Implement efficient fault simulation techniques
4. Design scan-based and BIST-based test architectures
5. Analyze test cost, coverage, and scalability
6. Apply testing concepts to modern systems (AI hardware, chiplets, AMS)

Topics:

1. Motivation - why test ?
2. Failure mechanisms and yield models
    - parametric vs. catastrophic faults
    - impact of scaled technologies
3. Theory of digital stuck-at fault testing -
    - basic concepts
    - fault excitation and sensitization
    - redundant faults and coverage
    - multiple faults
4. Circuit and fault simulation methods
    - digital circuits, parallel, deductive and concurrent
    - fault simulation
    - analog circuits
5. Test generation algorithms and test methods
    - digital, stuck-at and delay faults
    - analog/RF
    - delay fault testing
6. Memory Testing

7. Delay Testing and IDDq test method
8. Design for testability techniques
    - scan
    - JTAG, boundary scan
    - analog scan
    - test response compression
9. Built-in self-testable designs - pseudo-random tests
    - built-in test architectures
10. Self-calibration techniques
    - post manufacture circuit tuning for repair/yield-enhancement
11. New topics in test
    - analog/mixed-signal circuit testing
    - nanoelectronics test methods
    - testing of digital and analog hardware for artificial intelligence

Grading policy:

Test 1: 20%
Test 2: 20%
Final: 30%
HW: 5%
Project: 25%

Project: The project will involve writing a fault simulator and test vector generator for digital combinational circuits in a language of your choice. At the end of the semester, every student will be required to demonstrate both components of the project on "surprise" test cases that will be used to evaluate the correctness of the implemented algorithms.

Instructor contact information

The instructor, Prof. Chatterjee can be reached via e-mail: chat@ece.gatech.edu Please use the e-mail heading "ECE 6140" when communicating with the instructor throughout the semester.

Attendance policy:

The lectures will be recorded and will be available to both sections (in-class and video). However, for the in-class section, attendance will be required unless for medical and other personal reasons. Random attendance will be recorded and students with good or exceptional attendance will receive 1 or 2 extra points out of 100 (final total score).

Required course materials.

Textbook: Digital Systems Testing & Testable Design; Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman.

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. Review Georgia Tech's Honor Code https://catalog.gatech.edu/policies/honor-code/ and the student Code of Conduct https://catalog.gatech.edu/rules/18/ . Any student suspected of cheating or plagiarism on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services (404-894-2563) as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.

Student-Faculty Expectations Agreement

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. The Student-Faculty Expectations https://catalog.gatech.edu/rules/22/ articulate some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class