ECE 3030 Syllabus

Section A, 3 Credits
Fall 2026

Faculty Information

Instructor	Email
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General Course Information

Description

ECE 3030 explores the physical foundations of computation, where digital information is defined by binary node voltages established by the flow of electrons and holes. These charge carriers are regulated by transistors, which act as microscopic switches to either allow or block current, while metal interconnects facilitate the transfer of data across the chip. Long-term data storage is achieved through the physical trapping of electrons within dielectric layers, forming the basis for non-volatile memory.

Approximately sixty percent of the curriculum is dedicated to the metal-oxide-semiconductor field-effect-transistor, or MOSFET, which serves as the primary component of modern microelectronics. This section develops an understanding of semiconductor physics through concepts such as energy band diagrams, charge carrier density, and the mechanisms of drift and diffusion current. After establishing the physics of p-n junctions and MOS capacitors, the course introduces the CMOS inverter as the fundamental circuit primitive. This model allows for the analysis of energy dissipation and computation speed, providing a technical context for the relentless scaling and miniaturization that has driven the information technology revolution for over fifty decades.

The remaining forty percent of the course focuses on memory technologies, specifically examining the operation and architecture of SRAM, DRAM, and FLASH. Students investigate how different physical mechanisms allow for volatile high-speed access versus non-volatile long-term storage. If time permits, the course concludes with an overview of CMOS fabrication processes and an exploration of emerging paradigms. These advanced topics may include in-memory computing and neuromorphic architecture, which aim to move beyond traditional hardware limits to mimic biological processing.

Course Learning Outcomes

1. **Analyze Carrier Dynamics and Semiconductor Physics**: Transition from the bond model to the band model to describe electron and hole statistics and quantify carrier transport mechanisms through drift and diffusion.

2. **Understand Electrostatics**: Model the physical operation of a MOS capacitor and p/n junctions using band diagrams to explain electrostatic behavior perpendicular to the channel.

3. **Evaluate MOS Transistor Performance**: Derive and interpret Id-Vd and Id-Vg characteristic curves to understand transistor switching, including subthreshold swing and standby leakage current.

4. **Design CMOS Logic Gates**: Analyze the CMOS inverter to determine the Voltage Transfer Curve (VTC), calculate noise margins, and optimize for switching delay and energy dissipation.

5. **Explore Memory Architectures**: Compare and contrast the physical operation, density, and speed of dominant memory technologies, specifically SRAM, DRAM, and non-volatile FLASH.

6. **Understand Fabrication and Physical Design**: Apply knowledge of CMOS fabrication processes and EDA (Electronic Design Automation) flows to create physical layouts and understand the transition from planar transistors to FinFET architectures.

Required Course Materials

Textbook

- No official textbook is required

Supplementary Reading

- The following resources are recommended but do not need to be purchased

Modern Semiconductor Devices for Integrated Circuits

- **Author:** Chenming Calvin Hu
- **Publisher:** Pearson (2009)
- **Access:** A free download is available via the author's Berkeley website: https://www.chu.berkeley.edu/modern-semiconductor-devices-for-integrated-circuits-chenming-calvin-hu-2010/

Microelectronic Circuits (6th Edition)

- **Authors:** A.S. Sedra and K.C. Smith
- **Publisher:** Oxford University Press (2009)
- **Note:** Only three specific chapters from this text will be required.

Grading Policy

Your final grade will depend on the following combination of grades:

Homework (4 sets)	32%
Midterm 1	20%
Midterm 2	15%
Final Exam	33%

A: ≥ 90.0%
B: ≥ 80.0% and < 90.0%
C: ≥ 70.0% and < 80.0%
D: ≥ 60.0% and < 70.0%
F: < 60.0

Description of Graded Components

Final grades will be based on the weighted total.

Midterms: in class during first week of Oct & first week of Nov

Final exam: per Registrar's schedule.

Attendance and/or Participation

In-person class attendance is required but will not be checked
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Canvas Resources

- **PowerPoint lecture slides** will be posted on Canvas**.** I will post links and supplementary resources on Canvas. Class reminders and changes will be communicated via Canvas announcements
- **Course Schedule** located in the Canvas Syllabus Module.
- **Instructor Office hours:** Canvas Home Page
- **Teaching Assistant (TA) Office hours:** Canvas Home Page

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. Review Georgia Tech's Honor Code and the student Code of Conduct.

Any student suspected of cheating or plagiarism on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Accommodation for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services (404-894-2563) as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also email me as soon as possible in order to set up a time to discuss your learning needs.

Student-Faculty Expectations Agreement

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. The Student-Faculty Expectations articulate some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

Prerequisites

ECE 2020 **OR** ECE 2030

AND

ECE 2040

Extensions, Late Assignments, & Re-Scheduled/Missed Exams

Homework policy: All homework and assignments must be submitted by the established deadline. Late submissions will be subject to the following grading penalties:

- **Up to 24 hours late:** A **20% penalty** will be applied (score multiplied by 0.80).
- **24 to 48 hours late:** A **50% penalty** will be applied (score multiplied by 0.50).
- **Beyond 48 hours late:** A score of **zero** will be recorded.

Please note that any inquiries or disputes regarding the grading of homework or exams must be submitted within **one week** of the date the assignment was returned.

Make up exam policy: If you know you will miss an exam, please coordinate with Prof. Datta at least one week in advance to set up a time to take a makeup exam ahead of

the scheduled exam date. If you miss an exam without notifying Prof. Datta, you will receive a grade of 0 (zero) unless you have a legitimate reason for missing the exam. Examples of legitimate reasons to miss an exam include illness, illness or death in your immediate family, and participation in official university activities. **Documentation is required** for any exam to be considered excused; medical documentation should be submitted to the Dean of Students (https://studentlife.gatech.edu/request-assistance) and not to Prof. Datta. Makeup exams will be arranged **within 3 business days** of the missed exam.

Inclement Weather and Digital Learning Days

I will move the lecture to online, synchronous Teams session during inclement weather. I will communicate changes to class schedule using Canvas Announcement.

Student Use of Mobile Devices in the Classroom

Students may use mobile devices for instructional purpose. Laptops and iPads are permitted for taking notes if needed.

Undergraduate Student Academic Success Resources:

Academic Support: Academic Success and Advising (a unit in the Office of Undergraduate Education & Student Success) provides free support for your courses. Students can attend scheduled supplemental review (PLUS) sessions, stop by Drop-In Tutoring, or schedule a one-on-one appointment through Knack. To explore what options work best for you, please visit us online at success.gatech.edu/tutoring, email us at tutoring@gatech.edu, or come see us at Clough Undergraduate Learning Commons, Suite 283.

Student Well-Being:

"At Georgia Tech, we are concerned about your overall physical, social, and mental well-being." A comprehensive list of wellness related resources has been compiled and maintained by the Office of the Vice President for Student Engagement and Well-being (student-resource-guide (gatech.edu)