ECE4806/8806: Analog VLSI II – IC Validation and Characterization (Fall 2026)

Class time & location TBD

General Information

Instructor:

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Course Summary

ECE 4806/8806 VLSI-2 constitute a comprehensive Analog VLSI design experience for students involving theory, design, verification (in Analog VLSI-1) and test of a fabricated CMOS Analog VLSI design in (Analog VLSI-2). The centerpiece of this course is a semester-long effort by student-teams to combine basic principles Analog VLSI design with essential practices and principles that will allow a team of students to effectively validate and characterize both a packaged silicon sample chip, as well as directly on a wafer for the prototype they have themselves designed in VLSI-1. This syllabus outlines the second part of the two-semester series, which focuses on validation and characterization.

Upon successful completion of this course, students should be able to:

1. Given a test plan, suitably equip a workbench to perform chip testing, and write required programs in Python and C to generate test pattern for system validation and characterization.

2. Translate their understanding of hardware testing in the three various stages: Design (develop the test setup and solicit required components/instruments and prepare test PCB), Emulation (verify the test setup through a sample packaged chip) and finally Silicon Validation (develop and execute a wafer-level testing "bring-up" plan and translate the test setup to a commercial wafer level tester).

3. Design, organize, contribute to and run effective test reviews to identify operational anomalies. Propose underlying causes and develop a test-flow to investigate these proposed mechanisms.

4. Communicate analog prototype function and performance using industry-standard charts and formats (frequency spectrum plot, IND/DNL plots, dynamic range plots)

Prerequisites

ECE 4804/8804 AVS with a passing grade

Course Materials

Class Webpage
Canvas (https://canvas.gatech.edu/) is the primary means of distributing new information. **Homework assignments will be posted on Canvas and will not be handed out in class.** The following information will also be found on Canvas as it becomes available: (1) homework solutions, (2) tutorial materials, (3) class grades, (4) this syllabus, and (5) any supplementary materials relevant to this course.

On-Line Discussions
We will use **Piazza** (integrated in Canvas) to facilitate class discussions. We will try to check Piazza at least once a day. Please post questions about anything related to the course material, and also answer other students' questions, as long as you don't "give away the answer".

Textbooks
No textbook is required for this course. The instructor will rely on openly available reading-material that will be put together and made available on canvas.

Workload and Grading

Grading
Students in this course will be graded based on 4 components:

- In-class midterm (15%)
- Test assignments of known good chips (25%)
    - Team task 10%
    - Individual task 15%
- Individual evaluation board design (25%)
- Team test of their fabricated chip (25%)
- Class participation (10%)

The course is expected to be very strenuous. In accordance, grading policy is expected to be liberal. For instance, students with average performance in quizzes and homeworks and a fully functional, verified, robust final project should expect and "A" in this class.

Bonus credits will be offered on multiple occasions to incentivize students to adopt techniques/methodologies and develop valuable industry-relevant skills for improving design quality/productivity. Bonus credit will be awarded to provide a potential grade jump to students after initial bell-curve based grade-assignment.

Undergrad and grad session will be mainly differentiated through the efforts in the tape-out project. In this course, the project teams will be pre-formed to balance out the expertise such that each group's chance of success can be maximized. **Grad students will be assigned extra milestones, such as serving as chip captains.** For this reason, we require grad students taking the course to have higher technical readiness. A screening and selection process are thus required for grad students before they are permitted to enroll. Undergrad students and grad students will be graded separately.

Homework
Homework will take the form of team assignments, provided to students to develop their chip testing skills in the first half of the course. The objective of the assignments is to develop a firm grasp of (1) Basic functional test methodology; (2) Basic hardware characterization procedure; (3) Debug and hardware troubleshooting; Interpretation of measured silicon results.
IC design and test is a practitioner's art. Consequently, homework is not solely designed to facilitate mastering VLSI theory. Instead, homework is built to complement the theory taught in class to allow students to build hands-on techniques that are difficult to teach in a classroom setting. To complete these homework assignments, students will synthesize their (1) understanding of the theory covered in class lectures together with; (2) an ability to look through provided test plan and pattern generation documentation together with (3) skills they will develop to effectively manage multiple designs, files, and tools to produce robust, functional designs.

Course Expectations & Guidelines

Getting Help
The material in this course builds on earlier material, so it is very important to not get behind. Be sure to take advantage of office hours and other resources that are available. If you can't make office hours, email questions or arrange for an appointment.

Major Emergencies
If you have some sort of major life emergency – serious illness or injury, death in the family, house burns down or is flooded, etc. – that seriously impedes your progress in the class, please let us know as soon as possible so we can work something out. You will find professors can be quite reasonable if you keep us in the loop. Absence reporting procedures can be found in http://www.catalog.gatech.edu/rules/4/

On Things That Distract
Please silence all cell phones, tablets, pagers, etc. before entering class. If you forget to do so and receive a call, please shut the noisemaking device down as quickly as possible, and return the person's call *after* class. (Of course, there are reasonable exceptions for emergencies; in such cases leave your phone on vibrate, and answer it as quickly as possible and immediately step out of the room to handle the call.)

In general, please do not text, instant message, web surf, Facebook, tweet, e-mail, play games, etc. during class. It can be quite distracting. **Unless needed for class, the preferred position for laptops and tablets during class is in your backpack.**

Honor Code (http://www.policylibrary.gatech.edu/student-affairs/academic-honor-code)
Adherence to the Georgia Tech Honor Code is expected and all suspected instances of academic misconduct will be reported to the Dean of Students. It is your responsibility to ask for clarification if collaboration guidelines, test-taking policies, etc. are not clear.

Office of Disability Services (https://disabilityservices.gatech.edu/)
If you are a student registered with the Office of Disability Services (ODS), please make sure the appropriate forms and paperwork are completed by Prof. Li. We will abide by all accommodations required by ODS. It is the responsibility of the student to properly arrange test accommodations for each exam with ODS in sufficient time to guarantee space for exam administration. ALL exam accommodations must be

handled through ODS. If the student does not register accommodations with ODS for the taking of an exam, then they will have to take the exam at the normally scheduled times without any additional accommodation unless the instructor is given specific directive from ODS on the student's behalf due to a mitigating circumstance.

Student-Faculty Expectations Agreement
It is important to strive for an atmosphere of mutual respect and responsibility between faculty members and students. In the end, a respect for knowledge and understanding, an appreciation for hard work, and respectful interactions all contribute to an environment conducive to learning and excellence. I encourage you to remain committed to the ideals of Georgia Tech while in this class. See www.catalog.gatech.edu/rules/22 for a description of some basic expectations that we can have of each other.

Content Outline

The outline below is to be treated as an approximation. Since this is the first offering of its kind ever, some run-time adjustments will be inevitable.

1. PCB design with an emphasis on signal and power delivery from an analog IC's perspective.
2. Signal Integrity
3. Instrumentation fundamentals: signal generators, oscilloscopes, logic analyzers, spectrum analyzers
4. Test pattern generation for BIST and scan chain.
5. Identifying issues from measurement results
6. Wafer-level probing and testing