ECE 4452 Syllabus

Integrated Circuit Fabrication, 3 Credit Hours

Summer 2026

Instructor Information

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General Course Information

Description

This course covers the fundamental principles and techniques of integrated circuit fabrication. Topics include CMOS process flow, thermal oxidation, photolithography, diffusion, ion implantation, plasma etching and deposition, metallization, and fabrication and characterization of MOSFET, Inverter, Ring Oscillator, Nand and Nor gates. Students gain hands-on experience through weekly laboratory sessions in the cleanroom facility, where they fabricate actual CMOS devices from wafer preparation through device testing.

Course Learning Outcomes

Upon successful completion of this course, students should be able to:

- Describe the complete CMOS process flow and identify the role of each major fabrication step.
- Analyze thermal oxidation kinetics and apply the Deal-Grove model to predict oxide growth.
- Apply photolithography principles to understand pattern transfer and resolution limits.
- Evaluate diffusion and ion implantation as doping techniques and predict dopant profiles using simulation.
- Explain plasma processing, thin film deposition, and metallization methods used in IC manufacturing.
- Fabricate and characterize basic CMOS devices through hands-on cleanroom laboratory work.

Required Course Materials

Required textbook:

- G. May & S. Sze, Fundamentals of Semiconductor Fabrication, Wiley.

Recommended supplemental references:

- R. C. Jaeger, Introduction to Microelectronic Fabrication, 2nd ed., Prentice Hall.
- J. D. Plummer, M. Deal, and P. Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, Prentice Hall.

Grading Policy

Final grades will be determined on the following basis:

Component	Weight
Homework	15%
Midterm	30%
Final Exam	30%
Lab Reports	25%

Note: Final course grades are awarded on a scale of A–F with no +/− grades permitted.

Description of Graded Components

Exams (60%): There will be one midterm exam (30%) and one final exam (30%). The midterm will cover material from wafer characterization to SUPREME simulation. The final exam will be on material after the SUPREME chapter.

Homework (15%): Problem sets will be assigned throughout the semester to reinforce lecture material

Lab Reports (25%): Four or five lab reports are assigned on topics such as wafer characterization, oxidation, photolithography, diffusion and device characterization. Students are expected to maintain a laboratory notebook documenting all experimental observations, data, and analysis.

Course Policies

Attendance and/or Participation

Regular attendance is strongly encouraged for both lectures and laboratory sessions. Students are expected to attend all scheduled lectures and labs and are responsible for all material covered. Lab attendance is mandatory; if a student must miss a lab due to illness

or an approved Institute activity, they are responsible for contacting the instructor or lab instructor as soon as possible to arrange a make-up.

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. Review Georgia Tech's Honor Code and the student Code of Conduct.

Any student suspected of cheating or plagiarism on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Core IMPACTS

Not applicable

Accommodation for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services (404-894-2563) as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail the instructor as soon as possible in order to set up a time to discuss your learning needs.

Student-Faculty Expectations Agreement

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. The Student-Faculty Expectations articulate some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

Pre- & Co-Requisites

ECE 3040 (Introduction to Microelectronics) or equivalent, or instructor consent. Background in semiconductor device physics is recommended.

Laboratory Safety

All students must complete the required safety training before participating in any laboratory session in the cleanroom. A safety quiz will be administered during Week 1. Students who have not passed the safety quiz will not be permitted to enter the cleanroom. Proper personal protective equipment (PPE) must be worn at all times in the cleanroom. Any safety violations may result in immediate removal from the lab.

Collaboration, Group Work, and Use of Generative AI

All submitted homework must represent the student's own understanding. Lab reports should reflect each student's own analysis and interpretation of experimental results. In-class exams must be completed individually and are closed book and notes unless otherwise stated and an equation sheet will be provided.

Extensions, Late Assignments, & Re-Scheduled/Missed Exams

Late homework and lab report submission penalties are as follows:

- 1 day late: −20% of total assignment grade
- 2 days late: additional −10% (total −30%)
- No submissions accepted after two days past the due date

Make-up exams may be arranged for documented illness, approved Institute activities, or religious observances. Students must notify the instructor in advance whenever possible.

Course Outline

1. Introduction and Semiconductor Material Characterization

- Overview of IC fabrication and CMOS process flow
- Crystal structure of silicon; wafer preparation and characterization
- Cleanroom safety, protocols, and equipment overview
- Electrical and physical characterization techniques

2. Thermal Oxidation

- Oxidation mechanisms: dry and wet oxidation
- Deal-Grove model and oxide growth kinetics
- Oxide properties and characterization
- Role of oxide in CMOS: gate dielectric, isolation, masking

3. Photolithography

- Optical lithography principles and resolution limits
- Photoresist: positive and negative
- Exposure, development, and etching
- Alignment and overlay in multi-mask processes

4. Diffusion

- Fick's laws: pre-deposition and drive-in diffusion
- Gaussian and erfc dopant profiles

- Concentration-dependent and two-dimensional diffusion effects
- SUPREME process simulation

5. Ion Implantation

- Ion range and straggle; LSS theory
- Channeling and implant damage
- Annealing and dopant activation

6. Plasma Processing and Etching

- Plasma fundamentals: RF discharge and plasma chemistry
- Wet chemical and plasma etching: chemical, physical and reactive ion etching
- Selectivity and Isotropic vs. anisotropic etching
- Thin film deposition by CVD; APCVD, LPCVD and PECVD

7. Metallization

- Metal contacts interconnect requirements and materials
- Thin film deposition: evaporation and sputtering
- Al and Cu metallization
- Contact and via formation for multilevel metallization

8. Device Operation and Testing

- Operation and characterization of MOSFET
- Operation and characterization of Inverter
- Operation and characterization of Ring oscillator
- Operation and characterization of Nand and Nor gates
- Correlation of fabrication parameters with device performance