Processor Design

Course Information

Instructor: Yingyan Lin (ylin715@gatech.edu)
Course Prefix and Number: CS 3220 A
Term: Fall 2026

Course Description

This course introduces both traditional processor architectures and dedicated artificial intelligence (AI) accelerator architectures through lectures and hands-on laboratory work. As an intermediate-level course that follows CS 2200, it emphasizes the implementation of basic processor modules using Verilog and is designed to strengthen students' understanding of processor design, including pipeline design, operation parallelism, and on-chip communication protocols. Students also gain familiarity with Verilog programming and FPGA tool flow. Topics include hardware description language (Verilog), FPGA programming, pipeline design, parallel architecture design, NoC design, RISC-V processors, AI accelerators, Xilinx FPGA development tools, and Pynq boards.

Course Learning Outcomes

By enrolling in this course, students will:

1. Develop an understanding of foundational concepts in processor and accelerator design, including pipelining, operation parallelism, on-chip communication, NoC design, and RISC-V-based systems.

2. Gain experience in designing and implementing basic hardware modules using Verilog, FPGA programming workflows, Xilinx development tools, and Pynq boards.

3. Apply concepts from traditional processors and dedicated AI accelerators through hands-on laboratory assignments.

4. Strengthen debugging, testing, and iterative design skills while completing individual course work in accordance with course and academic integrity expectations.

Required Course Materials

Lecture notes are used throughout the course. Additional references are available online through the Georgia Tech library (http://library.gatech.edu/), including

1. Principles and Structures of FPGA (FPGA)
2. Quick Start Guide to Verilog (Verilog)
3. Computer Architecture: A Quantitative Approach (optional)

Grading Policy

This course is graded on a letter grade basis. Grading for the course will be broken down as follows:

Participation, Short Assignments, and Attendance	20%
Lab Assignments	80%
Entrance Exam	3% (bonus)
Total	**100% + 3% (bonus)**

Notes on Assignments:

- All assignments are due on the date and time specified in the assignment description and posted online. Late submissions are not accepted without prior approval.

- If an emergency or extenuating circumstance prevents a student from submitting an assignment by the deadline, the student should contact the Dean of Students' Office regarding the situation and class absence. The Dean of Students' Office can coordinate with students and alert instructors as appropriate. For anticipated conflicts that are unavoidable, such as weddings, business trips, or conferences, students should plan ahead and complete work before the due date.

- Students must follow the submission guidelines specified in each assignment description. Wrong file names, broken file formats, or missing files may result in a 5% grade deduction.

- Regrade requests must be submitted in writing to the instructor within one week of when the work was returned. If a lab is submitted for regrade, the instructor and TAs may regrade the entire assignment, and the score may increase or decrease.

Grade Scale

A 100%-90%
B 89%-80%
C 79%-70%
D 69%-60%
F <60%

Attendance Policy

This class is designed for students to become active participants, so it's vital that all students attend each class session and are fully engaged in all class activities. This means that you'll need to do more than just show up at the appointed time and place—you'll also need to come to class prepared to participate.

Please attend every scheduled meeting on time. That said, if you are exhibiting any symptoms of illness (fever over 100.4 F, coughing, nausea, etc.), please stay home to rest, seek medical attention if appropriate, and contact me as soon as possible. Excessive lateness and absences (3 or more per semester) can negatively impact your final grade outcome. If you have extenuating circumstances, the instructor will try and work with you to address those challenges. Please communicate early and often if you are struggling with issues that may call for accommodations.

Academic and Research Honesty/Integrity Statement

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. Review the Student Code of Conduct and the Academic Honor Code, especially Appendix A: Graduate Addendum to the Academic Honor Code.

Students are expected to perform research in an ethical and responsible manner. All Doctoral and Master's Thesis students are required to take the Responsible Conduct of Research training, and it is expected that students abide by the principles taught in that training while performing research for this thesis course.

Allegations of scientific or scholarly misconduct are handled in accordance with the procedures outlined by the Policy for Responding to Allegations of Scientific or Other Scholarly Misconduct.

Core IMPACTS

Not applicable.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.

Expectations of Advisors and Advisees

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. The Expectations of Advisors and Advisees articulates some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.