ECE 6465 Memory Device Technologies and Applications

Units: 3

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Course Description:

The functionality and performance of today's computer system is increasingly dependent on the characteristics of the memory components. This course covers the semiconductor memory technologies from the device bit-cell structures to the memory array design with an emphasis on the industry trend and cutting-edge technologies. The first part of the course discusses the mainstream semiconductor memory technologies that enable various levels in the memory hierarchy, including SRAM, DRAM, and NAND FLASH. Issues such as basic operation principles, device physics, manufacturing processes, bit-cell design considerations, array architectures and technology scaling trends will be discussed. The second part of the course discusses the emerging memory candidates that may have the potential to change the memory hierarchy, including RRAM, PCM, MRAM and FeFET/FeRAM, as well as their new applications such as in-memory computing for AI hardware.

Prospective Students:

Historically, the ECE curriculum emphasizes the logic components, e.g., the transistor technology at the device level, the digital VLSI design at the circuit-level, or the microprocessor at the architecture level. This course covers the overlooked part - the memory components, with a holistic view from the device level to the array level. Therefore, the students focusing on nanotechnology, VLSI systems and digital design may be interested in taking this course to broaden their skills and vision. The course is cutting-edge technology-oriented and driven by the industry trends, thus the students are expected to actively read the related literature as part of the learning process.

Course Objectives

As part of this course, students

- analyze the operations of a semiconductor memory bit-cell and its related stability, variability and reliability issues.
- analyze the operations of a memory array with peripheral circuitry with appropriate read/write timing and biases.
- analyze the scaling trend of the mainstream memory technologies.

- explore the new applications for the emerging memory technologies.
- utilize the design automation and simulation tools to analyze the memory-bit cell and peripheral circuitry design.

Learning Outcomes

Upon successful completion of this course, students should be able to

- Analyze and design of basic memory bit-cells including 6-transistor SRAM, 1-transistor-1-capacitor DRAM, and floating-gate/charge-trap FLASH transistor.
- Analyze and design of the peripheral circuits including the sense amplifier and array-level organization for the memory array.
- Understand the industry trend of the memory technologies such as FinFET/Nanosheet based SRAM, HBM, 3D V-NAND, etc.
- Assess the pros and cons of emerging memory technologies such as RRAM, PCM, MRAM and FeFET/FeRAM compared to the mainstream technologies.

Prerequisites

Undergraduate-level semiconductor device physics and digital integrated circuit design courses are strongly advised, e.g., ECE3040 Microelectronic Circuits, ECE3150 VLSI and Advanced Digital Design, or equivalents.

Assignments and Grading:

Homework 20%, 4 problem sets (5% each). Pre-knowledge about numerical tools such as MATLAB is required.

Lab (self-guided, computer based) 30%, 5 projects (6% each). Pre-knowledge about circuit simulators such as SPICE is required.

Midterm Exam 25%. Close book and close lecture notes, one cheat sheet and a calculator allowed in classroom setting. Midterm will be 75min in length in one of the regular class meeting time.

Final Exam 25%. Close book and close lecture notes, one cheat sheet and a calculator allowed in classroom setting. Final will be 90min in length in the Registrar scheduled final exam period.

No official textbook required; optional reference:

- S. Yu, **Semiconductor Memory Devices and Circuits**, Publisher: CRC Press/Taylor & Francis, 2022 (Available through GT library)

Notes/ Policy

- If you miss an exam without an approved absence (see Absence Policy below), you will get zero.
- If you turn in your homework/lab report after the deadline, your score will be multiplied by a factor of 80% within 24-hour late, 50% within 48-hour late, and zero beyond 48-hour late.

- Questions regarding homework/lab/exam grading must be asked within one week after the homework/exam is returned.

Academic Honor Code

The Honor Code applies to every aspect of this class, with only one noteworthy exception: student discussion of concepts and techniques for solving homework problems or lab projects is permitted outside the classroom. However, all the submitted work must be original and by individual. More details on academic honor code can be found at http://www.policylibrary.gatech.edu/student-affairs/academic-honor-code

Disability Accommodations

At Georgia Tech we strive to make learning experiences as accessible as possible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Office of Disability Services to explore reasonable accommodations. More details can be found at https://disabilityservices.gatech.edu/

Attendance and Absence Policy

The class will follow the Institute absence policy detailed at http://www.catalog.gatech.edu/rules/4/

Student-Faculty Expectations

The students and faculty instructor shall follow the expectations agreement set by the Institute detailed at

http://www.catalog.gatech.edu/rules/21/

Course Outline

- **Semiconductor Memory and CMOS Scaling Overview**
  - Introduction, industry trend, technology trend
- **SRAM**
  - 6T cell operation
  - Noise margin, stability, scaling issues, and layout
  - Variability and reliability issues
  - Recent trends: 8T cell, FinFET/Stacked nanosheet/Backside power delivery
- **DRAM**

  - 1T-1C cell operation
  - Fabrication technology, structure, layout
  - Recent trends: 3D TSV based DRAM, HBM, Monolithic 3D DRAM
  - Embedded DRAM (eDRAM)
- **FLASH memory**
  - FLASH device physics
  - NAND, NOR architecture
  - Reliability, scaling issues
  - Recent trends: 3D vertical NAND
- **Emerging memories**
  - Cross-point array architecture
  - RRAM
  - PCM
  - MRAM
  - Ferroelectric memories
- **Memory Array Design**
  - Peripheral circuits
  - Sense amplifiers
  - Bank-level simulator
- **New applications**
  - In-memory computing for AI hardware