ECE 4883/8883 Syllabus

Glass Core Packaging, Special Topics, and 3 Credits

Fall 2026

Instructor Information

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General Course Information

Description

Course Summary

Moore's Law has been a foundation for the semiconductor industry for more than 60 years enabling an unprecedent rate of improvement in monolithic integrated circuit (IC) performance and exponential increase in transistor density. However, due to several compounding effects, there is a very rapid and radical shift in the industry from the design and fabrication of complex monolithic ICs to heterogeneously integrated ICs. Where monolithic integration forms all circuit functions on a single common semiconductor (at the wafer scale), heterogeneous integration enables the concatenation of heterogeneous 'chiplets' of various functionalities (logic, I/O, memory, power conversion, passives, photonics, mm-wave, etc) and materials in a manner that mimics/exceeds monolithic-like performance and utilizing advanced off-chip '2.5D' and '3D' interconnects and packaging to provide flexibility in fabrication and design, improved scalability, reduced development time, and reduced cost. This new era of Moore's Law will be a game changer and will impact everybody.

The objective of this course is to introduce students to this 'new phase of Moore's Law' and to focus on the emerging field of glass-core packaging. This class will introduce students to various package substrate technologies, provide a detailed discussion of glass-core packaging processes and technologies through both lectures and labs, and introduce students to electrical and thermo-mechanical design considerations.

Course Learning Outcomes

Upon successful completion of this course, students will be able to:

1. Explain the role of glass core substrates in advanced electronic packaging and contrast them with organic and silicon interposers in terms of electrical, thermal, mechanical, and cost performance.
2. Describe and evaluate glass core fabrication processes, including through-glass via (TGV) formation, liner deposition, metallization, redistribution layers (RDL), and glass handling/processing challenges.
3. Analyze thermo-mechanical reliability issues in glass core packages, including CTE mismatch, stress evolution, warpage, fracture, and via reliability.
4. Apply electrical and signal-integrity principles to glass core packaging, including high-frequency loss mechanisms, impedance control, and interconnect parasitics.
5. Assess thermal management strategies for glass-based packages, including heat spreading, TIM selection, and package-to-system thermal resistance.
6. Utilize non-destructive and destructive characterization techniques (e.g., PLM, Raman spectroscopy, AFM, SEM, reliability testing) to evaluate glass cores, TGVs, and interfaces.
7. Design a glass core packaging solution for a target application (e.g., HPC, AI accelerators, co-packaged optics), considering integration, manufacturability, and reliability trade-offs.
8. Communicate technical findings effectively through written reports, presentations, and design reviews using professional engineering standards.

Required Course Materials

Fundamentals of Device and Systems Packaging: Technologies and Applications, Rao R. Tummala, McGraw-Hill Education; 2nd edition (September 2, 2019). Link to the Book online will be provided on the first day of class. More references will be given in the individual lectures

Course (ECE4883) Undergraduate Grading:

Homework: #1-3 18%

Reports: (Taking Notes in the labs is important)

Lab reports on the following topics (once in three weeks)

(Rubric will be provided)

a) Chip Embedding module 8%
b) RDL Module 8%
c) Assembly Module 8%
d) Electrical characterization module 8%

- Final Lab Report: 8%

Including introduction, reports a-d (report of different modules) and conclusion (including references)

Exams:

Exam 1: Lectures 1-12	20%
Exam 2: Lectures 13-24	20%
Attendance:	2%

Course Policies

Attendance and/or Participation

Grading includes:

Attendance:	2%

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. Review Georgia Tech's Honor Code and the student Code of Conduct.

Any student suspected of cheating or plagiarism on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services (404-894-2563) as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.

Student-Faculty Expectations Agreement

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student

body. The Student-Faculty Expectations articulate some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.