ECE/MSE/ME 6776: Microelectronics Systems Packaging
Fall 2026

Instructor: Prof. Muhannad Bakir (ECE)
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Office: Marcus 4135
Office Hours: Tuesday, 10-11 AM
TA: TBD
Class time: MW 2:00 - 3:15 PM @ Manufacturing Related Disciplines Complex 2404

Course Overview:
Course overview: Monolithic silicon integrated circuits (ICs) have progressed at an unprecedented rate of innovation in the past 60 years through Moore's Law. During much of these 60-years, electronic packaging played a 'secondary-role' – the package was there to enable simple space transformation and routing of interconnects off-chip. This, however, has changed. Today, advanced packaging and heterogeneous integration have evolved to be critical enablers to the next phase of Moore's Law. It is widely accepted that classical monolithic integration can no longer simultaneously meet performance, power, and cost needs of future electronics, and thus, giving rise to the ever more critical fields of "advanced packaging" and "heterogeneous integration." In this class, we explore traditional packaging technologies and emerging new heterogeneous integration architectures based on 2.5D and 3D integrated circuits. This class will explore these important new integration technologies along with understanding some of the electrical, thermal, and thermo-mechanical design considerations. The course material is both very timely and exciting given the revolutionary changes happening today in IC design and technology.

Course Outcomes:
Upon successful completion of this course, students should be able to:

1) Explain the interaction between ICs and advanced packages
2) Explain the fundamentals of advanced packaging technologies, including process flows
3) Design and model transmission lines in package substrates
4) Explain differences between interconnect technologies and their electrical design considerations
5) Explain thermal challenges in advanced packaging; perform thermal modeling
6) Become versed in Ansys HFSS (High-Frequency Structure Simulator)
7) Explain advanced packaging needs for various applications that include digital, RF/mm-wave, and photonics

We will accomplish these objectives through a combination of homework, quizzes, and projects.

Text Book:
- Fundamentals of Device and Systems Packaging: Technologies and Applications, 2nd Edition, Rao Tummala; (Available online through GT Library [AccessEngineering Database])
- Will supplement the course with journals and conference proceedings

Grading:
Homework: 15% (graded based on effort)
Exams: Two in-class exams each 30% (60% total)
Project: 25%

Exams: There will be two exams during the semester. All exams are closed book and closed notes. You may bring one US letter page (8.5 by 11 inches, one side) of **handwritten** notes and formulas to each of the two exams (along with a scientific calculator).

Project: ***Advanced Package Design***

The goal of the class project is to design an advanced package with multilayer interconnects to meet electrical, thermal, and manufacturing requirements. The design will leverage commercial software packages that we will learn in class. We will investigate the impact of different dielectrics, interconnect dimensions, substrate materials, assembly among other considerations on the performance of the advanced package and its manufacturability. More details will be provided during the semester. The total project grade will be split into three parts:

20%: Survey of state-of-the-art advanced packages (2 pages)

65%: Modeling, simulation, and optimization (4 pages)

15%: Discussion of the manufacturing constraints and recommended tools/processes (1 page)

Course Topics Include:

- Traditional interconnection approaches: wirebonds and flip-chip
  - Traditional packaging
  - Discuss technology and pros/cons
  - Electrical and thermal design considerations
  - Material attributes
  - Fabrication and processes
- Package substrates
  - Organic
  - Ceramic
  - Glass
  - Silicon
  - Polymer (flexible electronics)
- Emerging 2.5D and 3D IC Technologies
  - Discussion of technology options (bridge-chip, interposer, etc)
  - State of the art (products and research)
  - Fabrication and technology considerations
    - TSVs
    - Polymer bonding

        - Oxide bonding
        - Cu-Cu
        - Hybrid bonding
    - Fan-out wafer-level packaging
    - Electrical modeling
        - Parasitics
        - S-parameters; [RLCG] extraction
        - HFSS overview and modeling
        - Various interconnect technology modeling and benchmarking
        - High bandwidth density digital signaling design considerations
        - Power delivery design considerations
- Thermal challenges and opportunities
    - Thermal modeling
    - Impact of temperature on electronics
    - Overview of cooling technologies (conductive and convective) and benchmarking
    - State of the art demonstrations/products
- RF/mm-wave and photonic packaging
    - Unique challenges
    - Design considerations
    - Material properties
    - Examples of state of the art
- Thermomechanical design considerations
    - Materials, stresses, warpage in 2.5D and 3D IC technologies

Projected course schedule is shown below. Please note that the dates of the industry guest speakers are tentative.

Week	Topic	Notes
24-Aug	Welcome and Introduction to the Field	
31-Aug	Packaging Technology Evolution: Wirebonds, Surface-Mount, Flip-Chip	
7-Sep	**Monday: Holiday** [Cont.] Packaging Technology Evolution: Wirebonds, Surface-Mount, Flip-Chip	Holiday: Monday Sept. 7th
14-Sep	Electrical Design Consideration for Electronic Packages	
21-Sep	HFSS Demo: Modeling Wirebonds, flip-chip, and redistributions layers	
28-Sep	[cont.] HFSS Demo: An example Multi-layer Package with Microvias Substrate Technologies: Organic	
5-Oct	**Monday: Fall Break** [cont.] Substrate Technologies: Glass-Core and Bridge-Chip Technologies	Fall Break: Oct. 5-6
12-Oct	3D ICs: Through-silicon vias [Processes and Modeling]	Quiz 1 on Wednesday Oct. 14th
19-Oct	[cont.] 3D ICs: Through-silicon vias [Processes and Modeling]	
26-Oct	3D IC: Bonding and Integration Technologies, Including Interposers	Project State-of-the-Art Survey Due Wed. Oct. 29th October 31: Withdraw deadline
2-Nov	Thermal Design &Technologies	
9-Nov	[cont.] Thermal Design, Technologies and Examples Thermomechanical Design of Electronic Packages	
16-Nov	[cont.] Thermomechanical Design of Electronic Packages **Quiz 2 on Wednesday**	Quiz 2 on Wednesday Nov. 18th
23-Nov	Advanced Packaging Lab Tour **Wednesday: Student Recess**	Wednesday Nov. 25: Student Recess
30-Nov	Industry Guest Lecture Industry Guest Lecture	
7-Dec	Final project discussion [No Final Exam; project due]	

Attendance and Participation:
While attendance will not be considered as part of your grade, active participation and engagement with course materials, discussions, and activities are strongly recommended to facilitate your learning and success in this course. The instructor reserves the right to give bonus points on any day to course attendees.

Accommodations for Individuals with Disabilities:

If you are a student that requires special accommodations, please contact the Office of Disability Services at (404)894-2563 or http://disabilityservices.gatech.edu/. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs and how I can support you.

Academic Integrity:
Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. For information on Georgia Tech's Academic Honor Code, please visit http://www.catalog.gatech.edu/policies/honor-code/ or http://www.catalog.gatech.edu/rules/18/. Any student suspected of cheating or plagiarizing on a quiz, project, or assignment will be reported to the Office of Student Integrity.

Student-Faculty Expectations Agreement:
At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.